Quiz 3

1. Draw Mixed-Logic Circuit Diagram
2. Create Truth and Voltage Table

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **/B** | **/C** | **A\*/C\*D** | **A\*/B\*C\*D** | **/C\*D** | **Y** |
| 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

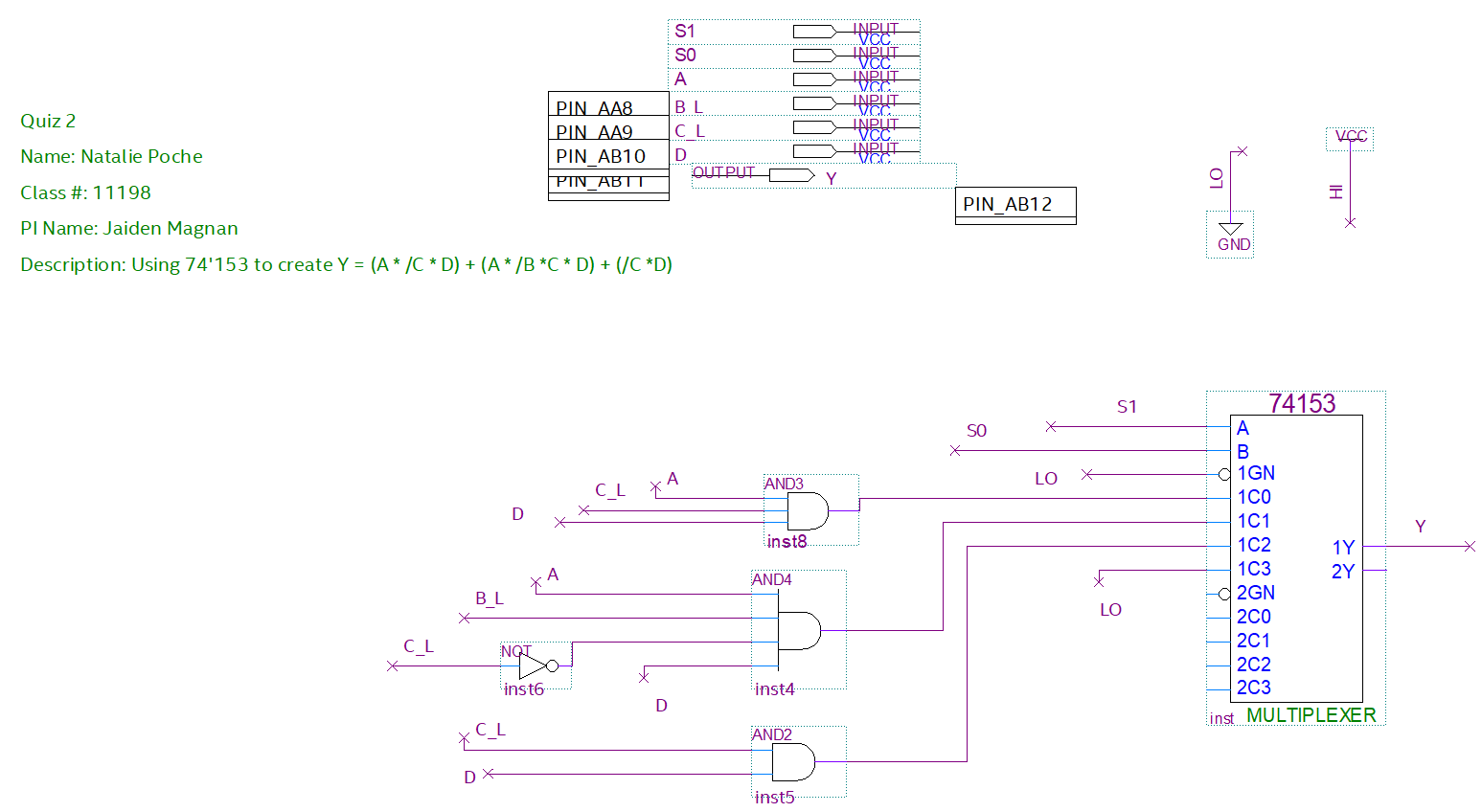
Figure : Truth Table for Y = A\*/C\*D + A\*/B\*C\*D + /C\*D

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **C** | **D** | **/B** | **/C** | **A\*/C\*D** | **A\*/B\*C\*D** | **/C\*D** | **Y** |
| L | L | L | L | H | H | L | L | L | L |
| L | L | L | H | H | H | L | L | H | H |
| L | L | H | L | H | L | L | L | L | L |
| L | L | H | H | H | L | L | L | L | L |
| L | H | L | L | L | H | L | L | L | L |
| L | H | L | H | L | H | L | L | H | H |
| L | H | H | L | L | L | L | L | L | L |
| L | H | H | H | L | L | L | L | L | L |
| H | L | L | L | H | H | L | L | L | L |
| H | L | L | H | H | H | H | L | H | H |
| H | L | H | L | H | L | L | L | L | L |
| H | L | H | H | H | L | L | H | L | H |
| H | H | L | L | L | H | L | L | L | L |
| H | H | L | H | L | H | H | L | H | H |
| H | H | H | L | L | L | L | L | L | L |
| H | H | H | H | L | L | L | L | L | L |

Figure : Voltage Table for Y = A\*/C\*D + A\*/B\*C\*D + /C\*D

L

1. BDF Quartus Circuit Design



1. Simulation results

